Ldic™
Semiconductor Solution
For Mass Storage

LD4200
NEWPORT
Advance Information

FEATURES

General

- 100 - 550 Mb/sec data rate operation
- Extended Class 4 Partial Response with Viterbi detection (EPRML) system
- Rate 16/17 Trellis Constraint code (32/34 endec) with Post-Processor
- Robust frame synchronization
- Support OKC dual sync byte and TCO direct write with LV diff input
- Code violation flag
- Programmable continuous-time + adaptive boost equalization
- Programmable write precompensation
- Thermal asperity detection and compensation for MR heads
- Adaptive compensation for MR head amplitude asymmetry
- 3 Taps Cosine Equalizer
- 8-bit NRZ interface
- 3-wire serial port for parameter and mode control
- 3.3V (±5%) power supply
- Power management
- Less than 15 mW during power down mode
- 0.25 μm technology

Equalization

- 7-th order equiripple continuous-time filter with programmable cut-off frequency, boost, and asymmetry of zeros. On-chip functions to assist in the selection of the filter parameters for equalization to EPR4 target pulse response.
- Adaptive boost control for equalizing amplitude distortion.

Automatic Gain Control

- Decision-directed digital acquisition and tracking loops.
- Fixed gain mode with programmable gain range of 0.25 to 4.0 using 8-bit DAC. Steps are equally spaced in 0.1 dB/lsb.
- Two additional gain range settings: Low gain mode decreases the gain range by 4.5dB. High gain mode increases the gain range by 4 dB.
- Programmable Viterbi gain with values from 1-6/32 to 1+6/32 in 1/32 steps.

Timing Recovery

- Decision-directed digital timing recovery for both acquisition and tracking modes.
- Zero phase startup for rapid acquisition.

ML Detector

- 8-state Viterbi detector for EPR4 target response.
- Marginalized data available for use in margin-type (stress) testing.

Data Separator

- Robust frame synchronization. Programmable time-out and programmable error tolerance on sync byte detect.
- Single byte sync byte indicator.
- 100 to 550 Mb/sec operation.

Frequency Synthesizer

- Independent “divide-by” registers for reference frequency and VCO output frequency.
- 10 to 60 MHz reference clock.
- 3-to-1 range with better than 1% resolution.

Write Mode

- Preamble is written immediately after activation of Write Gate (WG) (active high).
- CIA write mode: writes the preamble, sync byte, and PRBS pattern.
- Immediate direct write mode: bypass preamble, sync byte, encoder and precoder.
- Programmable precompensation of up to 35% of the write bit interval in approximately 1.13% steps to compensate for transition-shift distortion.
- Squelch VGA input during write mode (AGC is held). Squelch duration after deactivation of WG is programmable using WGDLY(register TA2, 0x7c[7:5]) from 0 to 56*TFREF1 µsec steps (TFREF1 = one period or half period of FREF clock).

Read Mode

- CIA read mode: bypass decoder and precoder.
- Pipeline read feature.
- Adaptive compensation of MR head amplitude asymmetry.
- Adaptive compensation of DC offset in ADC.
- Thermal asperity detection/correction.
- On-chip programmable noise generator to accelerate bit error rate tests.

Channel Integration Assist (CIA)

- Sum-of-squared error output register for measuring signal quality and selecting equalizer parameter settings. Register is reset after each fetch.
- Surface defect scan with provision for defining separate positive and negative amplitude qualification thresholds.
- Frequency indicator for VCO center frequency calibration.
- On chip BER capability.

Servo

- Asynchronous Digital Servo