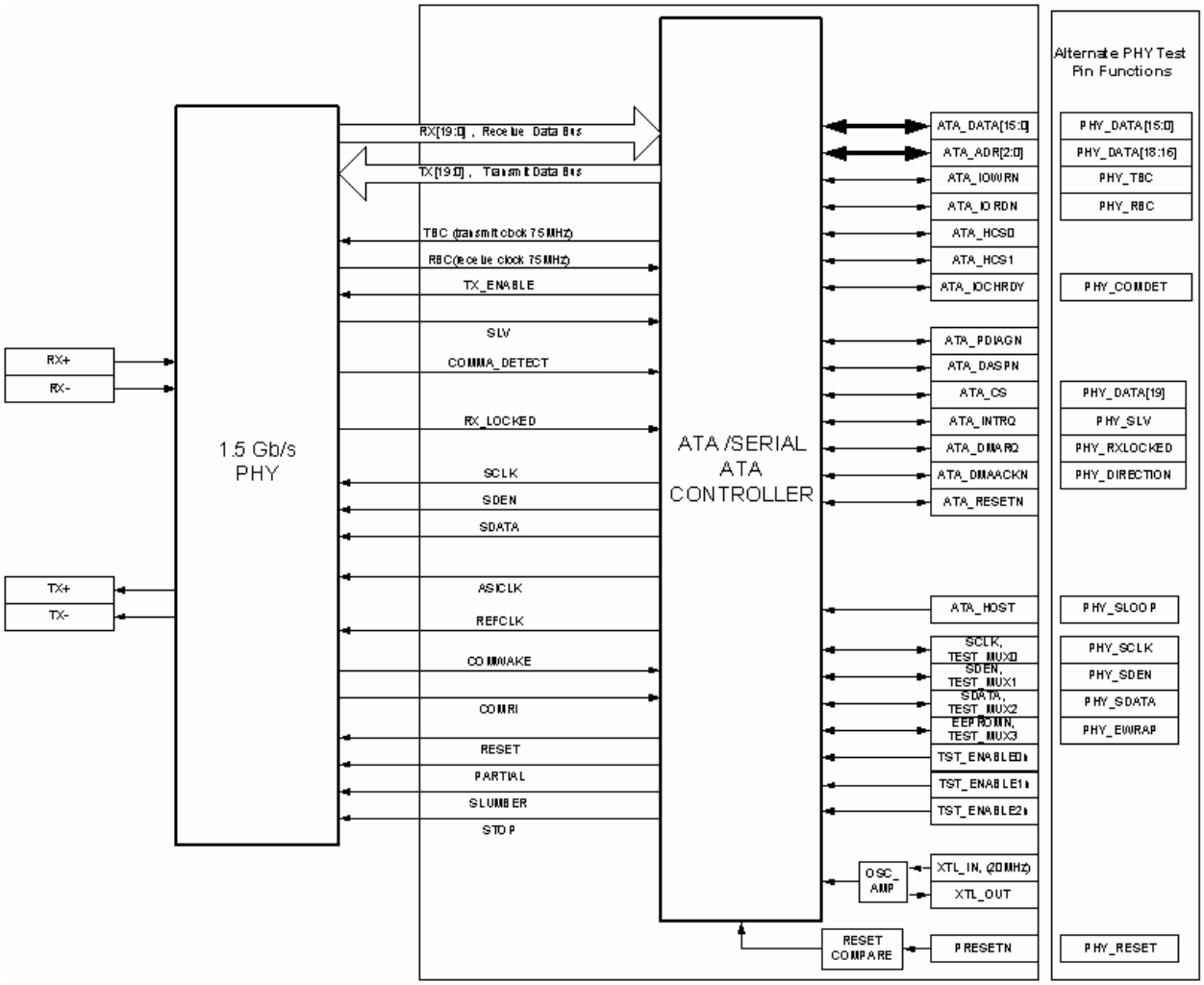
General Description:

The LDIC's Serial ATA IP Core, LD-LLC-0001-050 provides link and transport layers. This macro is fully compliant to Serial ATA Gen.1. The bridge is intended to adapt an ATA 66, ATA 100, ATA 133, and ATA 150 Disk drive to a Serial ATA Host or Parallel host to serial ATA interface. The Parallel ATA block connects directly to an IDE HOST or an IDE DEVICE (or target). The PHY interface is based on an industry standard XGMII interface definition with some additional signals for usage in the Serial ATA environment.

The PHY is connected to the ATA block of the IP by using the 20 bit transmit and separate 20 bit receive data bus. These two buses are sampled on the transmit clock (TBC) and the receive clock (RBC). Both PHY and the ATA/Serial ATA blocks can be tested individually or together. This is accomplished with the TEST_MUX and TEST_ENABLEN pins on the device.

Features:

- Verliog RTL codes
- Estimated gate count 50K
- Serial ATA rev1 compliant – Generation 1 Host and Device.
- ATA6 compliant Drive interface Host and Device.
- Supports 66MHz, 100MHz, 133MHz and 150MHz parallel ATA speed.
- Parallel ATA HOST to Serial ATA Interface
- Serial ATA to Parallel ATA Device Interface
- Serial interface to external serial EEPROM
- Big Drive Interfacing- 48 bit block Addressing.
- OOB COMRESET and COMAWAKE Detection.
- OOB COMINIT and COMWAKE Generation.
- 8B/10B Encoding and Decoding.
- Separate Cont and Data Scramblers to reduce EMI
- 32 bit Internal Buses for Encoding/Decoding/CRC Generating/Checking and Scrambling.
- Ultra-DMA with separate 16 bit CRC Generator.
- Primitive Decoder with auto Task File Updating.
- Dual 1024 byte Transmit/Receive FIFO's for over run prevention.
- Auto Inserted Hold Primitives to prevent under runs.
- Power Monitor for glitch free Power Off/On cycles.
- Power management modes (Partial and Slumber).



Block Diagram